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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/470,265	12/22/99	ROBINSON	K 303.455US3

EXAMINER	
NGUYEN, C	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/470,265	ROBINSON
Examiner	**Group Art Unit**
CUONG Q NGUYEN	2811

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

P ri d f r R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 19-20, 53, 79-87, 98-102, 104-118 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 19-20, 53, 79-87, 98-102, 104-118 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ Th proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ Th drawing(s) filed on_____ is/are objected to by the Examiner.

☐ Th specification is objected to by the Examiner.

☐ Th oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Ref rence(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing R view, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other_____

Office Action Summary

U. S. Patent and Trademark Office
PTO-326 (Rev. 9-97)

Part of Paper No. M

*U.S. GPO: 1998-454-457/97505

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 79, 82, 83, 86, 104, 105, 106, 113, 114, 115, 116, 117, 118, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "a first conductive plate formed from at least one metal selected from the group consisting of titanium, copper, gold, and nickel, alloy at least on additional metal selected from the group consisting of strontium, barium, and lead.....a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate." is not described in Fig.1 to Fig.7 and in the original specification. Applicant says that "first conductive 25, preferably a polysilicon layer" (page 4 of specification) and "first conductive layer may actually be comprised of more than one material. For example in a ministack application a conductive plug and further conductive layers overlying the conductive plug may form the first conductive layer. Nowhere in the original specification or in the drawings teaches that " the first

conductive plate formed by an alloy of Ti (or copper, gold, nickel) with Sr (or barium, lead)" and "a dielectric layer formed between first and second conductive plates, wherein the dielectric layer is an oxide of a metal layer on the first conductive plate".

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 19, 53, 79, 81, 85, and 87 insofar in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida (US 6,051,885).

Yoshida discloses DRAM memory device including a capacitor structure comprising: a first conductive plate (12 a lower capacitor electrode formed of tungsten such as tungsten); a metal layer (18) formed on the first conductive plate; a second conductive plate (24, an upper capacitor electrode formed of metal or polysilicon) formed on the first conducive plate; a dielectric layer (22, a metal oxide layer formed by oxidizing the metal layer) formed between the first and second conductive plates. See Yoshida's Fig.12A and col.9 lines 12-22.

Claims 19, 53, 80-81, 85-87, 104, 106-107, 111-114, and 117-118 insofar in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 102(a) as being anticipated by Bronner et al. (US 5,876,788).

Regarding claims, 19, 53, 79, 80, 81, 85, 86, 87, 104, 106, 107, 108, 111, 113, 117, Bronner et al. discloses DRAM memory device including a capacitor structure comprising: a first conductive plate (12, a lower capacitor electrode formed of doped silicon); a metal layer (16, a layer of Ti or an alloys of Ti and strontium, barium, lead. See Bronner et al.'s col.4, lines 20-30) formed on the first conductive plate; a second conductive plate (24, an Al upper capacitor electrode) formed on the first conducive plate; a dielectric layer (22, a metal oxide layer formed by oxidizing the metal layer) formed between the first and second conductive plates. See Bronner et al.'s Fig.1(b) and Fig.2(a).

Regarding claims 112, 114, and 118, as shown in Bronner et al.'s Fig.1(b), an oxidation resistant layer (14, a silicon nitride layer) formed between the first conductive plate (12) and the metal layer (16).

Claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 insofar in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 102(a) as being anticipated by Zahurak et al. (US 5,960,294).

Regarding claims, 19, 53, 79-81, 85-87, 98-102, 104, 106, 107, 108, 111, 113, 117, Zahurak et al. discloses a DRAM memory device including a capacitor structure

comprising: a substrate (11); an insulating layer (12) formed on the substrate; a contact hole formed in the insulating layer to expose a portion of substrate; a first conductive layer (18 and 20, a polysilicon lower capacitor plate) formed in the contact hole and contact to the substrate, a capacitor dielectric layer (24, a barium strontium titanate layer, a metal oxide layer including titanium, barium, strontium. See Zahurak et al.'s col.5, lines 45-52) formed on the first conductive layer; and a second conductive layer (26, a polysilicon or metal layer) formed on the capacitor dielectric layer. See Zahurak et al.'s Fig.1F.

Regarding claims 112, 114, and 118, as shown in Zahurak et al.'s Fig.1F, an oxidation resistant layer (22, a silicon nitride layer) formed between the first conductive plate (12) and the dielectric layer.

Claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 insofar in compliance with 35 U.S.C 112 are rejected under 35 U.S.C. 102(a) as being anticipated by Bronner et al. (US 5,876,788).

Regarding claims, 19, 53, 79-81, 85- 87, 104, 106, 107, 108, 111, 113, 117, Bronner et al. discloses DRAM memory device including a capacitor structure comprising: a first conductive plate (12, a lower capacitor electrode formed of doped silicon); a metal layer (16, a layer of Ti or an alloys of Ti and strontium, barium, lead. See Bronner et al.'s col.4, lines 20-30) formed on the first conductive plate; a second conductive plate (24, an Al upper capacitor electrode) formed on the first conducive

plate; a dielectric layer (22, a metal oxide layer formed by oxidizing the metal layer) formed between the first and second conductive plates. See Bronner et al.'s Fig.1(b) and Fig.2(a).

Regarding claims 112, 114, and 118, as shown in Bronner et al.'s Fig.1(b), an oxidation resistant layer (14, a silicon nitride layer) formed between the first conductive plate (12) and the metal layer (16).

The cited process limitations in claims 98-102 and limitations "a dielectric is an oxide of a metal layer overlying the first conductive plate" and "a dielectric formed by oxidizing a metal layer overlying the first conductive plate" in claims 19, 20, 53, 98, 104, 105, and 106 are taken to be a product by process limitation. For example, the final structure of the dielectric layer can be formed by different processes such as the dielectric layer can be formed by depositing a metal oxide layer on the first conductive plate of can be formed by depositing a metal layer on the first conductive plate and then oxidizing the metal layer. It is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292

(Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 82-84, 105, 109, 110, 115, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahurak et al.

Zahurak et al. teaches all limitations of claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 above. However, Zahurak et al. does not explicitly teach that the DRAM device is a portion of a monolithic memory device in a memory system, wherein a processor configured to access the monolithic memory device.

It would have been obvious to one of ordinary skill in the art to incorporate Zahurak et al.'s DRAM memory device in the memory system as claimed because the memory structure such that the DRAM device is a portion of a monolithic memory

device in a memory system, wherein a processor configured to access the monolithic memory device is conventional and well known in the art.

Claims 20, 82-84, 105, 109, 110, 115, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronner et al.

Bronner et al. teaches all limitations of claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 above. However, Bronner et al. does not explicitly teach that the DRAM device is a portion of a monolithic memory device in a memory system, wherein a processor configured to access the monolithic memory device.

It would have been obvious to one of ordinary skill in the art to incorporate Bronner et al.'s DRAM memory device in the memory system as claimed because the memory structure such that the DRAM device is a portion of a monolithic memory device in a memory system, wherein a processor configured to access the monolithic memory device is conventional and well known in the art.

Claims 98-102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. in view of Jost et al. (US 5,563,089).

Bronner et al. teaches all limitations of claims 19, 53, 79-81, 85-87, 104, 106-107, 111-114, and 117-118 above. However, Bronner et al. does not explicitly teach that the lower capacitor having container structure formed in a contact hole of an insulating layer overlying a substrate.

Jost et al. discloses a DRAM memory device including a container capacitor structure comprising: a substrate (11); an insulating layer (28) formed on the substrate; a contact hole formed in the insulating layer to expose a portion of substrate; a polysilicon layer (36, a lower capacitor plate) formed in the contact hole and contact to the substrate, a capacitor dielectric layer (38) formed on the polysilicon layer; and an electrically conductive layer formed on the capacitor dielectric layer. See Jost et al.'s Fig.2 to Fig.7.

It would have been obvious to incorporate the container capacitor having a lower capacitor in the insulating layer as taught by Jost et al. into Bronner et al.'s device in order to increase cell capacitance. See Bronner et al.'s col.1, lines 20-43.

Response to Arguments

4. Applicant's arguments with respect to claims 19-20, 53, 79-87, 98-102, and 104-106 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

CN

June 6, 2001

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER